REMARKS

Additional claims have been added which reflect what was set forth in the originally filed application. Further, the specification has been amended to conform with the figures, as originally filed. No new matter has been added.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100.

Respectfully submitted,

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Appendix A

LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

~~METHOD AND APPARATUS FOR A LIGHTING MODULE IN A GRAPHICS PROCESSOR~~

RELATED APPLICATIONS

The present application is related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 06, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed under attorney docket number NVIDP006, "Method, Apparatus and Article of Manufacture for Clip-less Rasterization using Line Equation-based Traversal" which was filed under attorney docket number NVIDP007, "A Transform, Lighting and Rasterization System Embodied on a Single Semiconductor Platform" which was filed under attorney docket number NVIDP008, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed under attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture for a Transform Module in a Graphics Processor" which was filed under attorney docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Independent Execution Threads" which was filed under attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.

~~The present application is related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 06, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed under attorney docket number NVIDP006, "Method, Apparatus and Article of Manufacture for Clip-less Rasterization using Line Equation-based Traversal" which was filed under attorney docket number NVIDP007, "A Transform, Lighting and Rasterization System Embodied on a Single Semiconductor Platform" which was filed under attorney docket number NVIDP008, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed under attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture for a Transform Module in a Graphics Processor" which was filed under attorney docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Independent Execution Threads" which was filed under attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.~~

FIELD OF THE INVENTION

The present invention relates generally to graphics processors and, more particularly, to a lighting module of a graphics pipeline system.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects and advantages are better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 illustrates the prior art;
~~Figure 1 illustrates a prior art method of rasterization;~~

Figure 1A is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;
~~Figure 1A illustrates the association of a set of edge variables with a particular pixel in accordance with a prior art method of rasterization;~~

~~Figure 1B is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;~~

Figure **2** is a schematic diagram of a vertex attribute buffer (VAB) in accordance with one embodiment of the present invention;

Figure **2A** is a chart illustrating the various commands that may be received by VAB in accordance with one embodiment of the present invention;

Figure **2B** is a flow chart illustrating a method of loading and draining vertex attributes to and from VAB in accordance with one embodiment of the present invention;

Figure **2C** is a schematic diagram illustrating the architecture of the present invention employed to implement the operations of Figure **2B**;

Figure **3** illustrates the mode bits associated with VAB in accordance with one embodiment of the present invention;

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 illustrates the prior art. Figures 1A - 32C show a graphics ~~Figures 1 and 1A show the prior art. Figures 1B - 32C show a graphics~~ pipeline system of the present invention. ~~pipeline system of the present invention~~.

Figure 1A is a flow diagram illustrating the various components of ~~Figure 1B is a flow diagram illustrating the various components of one~~ embodiment of the present invention. As shown, the present invention is ~~embodiment of the present invention. As shown, the present invention is~~ divided into four main modules including a vertex attribute buffer (VAB) 50, ~~into four main modules including a vertex attribute buffer (VAB) 50, a transform~~ a transform module 52, a lighting module 54, and a rasterization module 56 ~~module 52, a lighting module 54, and a rasterization module 56 with a set-up module~~ with a set-up module 57. In one embodiment, each of the foregoing modules ~~57. In one embodiment, each of the foregoing modules is situated on a single~~ is situated on a single semiconductor platform in a manner that will be ~~semiconductor platform in a manner that will be described hereinafter in greater~~ described hereinafter in greater detail. In the present description, the single ~~detail. In the present description, the single semiconductor platform may refer to a~~ semiconductor platform may refer to a sole unitary semiconductor-based ~~sole unitary semiconductor based integrated circuit or chip.~~ integrated circuit or chip.

The VAB **50** is included for gathering and maintaining a plurality of vertex attribute states such as position, normal, colors, texture coordinates, etc. Completed vertices are processed by the transform module **52** and then sent to the lighting module **54**. The transform module **52** generates vectors for the lighting module **54** to light. The output of the lighting module **54** is screen space data suitable for the set-up module which, in turn, sets up primitives. Thereafter, rasterization module **56** carries out rasterization of the primitives. It should be noted that the transform and lighting modules **52** and **54** might only stall on the command level such that a command is always finished once started.

In one embodiment, the present invention includes a hardware implementation that at least partially employs Open Graphics Library (OpenGL®) and D3D™ transform and lighting pipelines. OpenGL® is the computer industry's standard application program interface (API) for defining 2-D and 3-D graphic images. With OpenGL®, an application can create the same effects in any operating system using any OpenGL®-adhering graphics adapter. OpenGL® specifies a set of